TITLE: PROGRAMMING OF A FLASH MEMORY CELL
INVENTOR(S): Sheung Hee Park, Wing Han Leung, and Richard M. Fastow
USSN: 10/617,971   Attorney Docket #: AMD-H0523

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FIGURE 1A
(CONVENTIONAL ART)

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USSN: 10/617,971   Attorney Docket #: AMD-H0523

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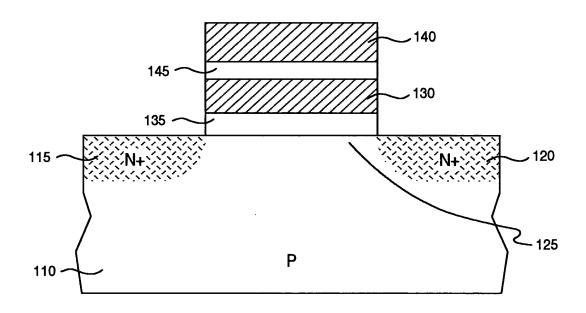
BITS

00 ———————————————— $V_{T3} = 7V$

01 ———————————————— $V_{T2} = 5V$

10 ———————————————— $V_{T1} = 3V$

11 ———————————————— MIN $V_T = 1V$

FIGURE 2A
(CONVENTIONAL ART)

BITS

000 ———————————————— $V_{T7} = 8V$

001 ———————————————— $V_{T6} = 7V$

010 ———————————————— $V_{T5} = 6V$

011 ———————————————— $V_{T4} = 5V$

100 ———————————————— $V_{T3} = 4V$

101 ———————————————— $V_{T2} = 3V$

110 ———————————————— $V_{T1} = 2V$

111 ———————————————— MIN $V_T = 1V$

FIGURE 2B
(CONVENTIONAL ART)

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FIGURE 3

(CONVENTIONAL ART)

FIGURE 4

(CONVENTIONAL ART)

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FIGURE 5
(CONVENTIONAL ART)

TITLE: PROGRAMMING OF A FLASH MEMORY CELL
INVENTOR(S): Sheung Hee Park, Wing Han Leung, and Richard M. Fastow
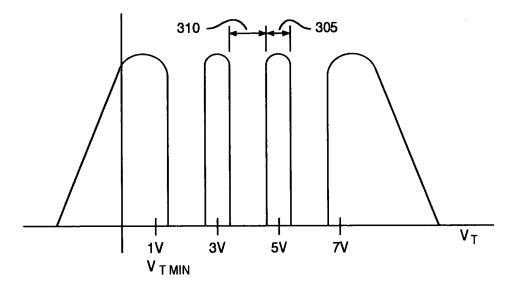USSN: 10/617,971   Attorney Docket #: AMD-H0523

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FIGURE 6

TITLE: PROGRAMMING OF A FLASH MEMORY CELL
INVENTOR(S): Sheung Hee Park, Wing Han Leung, and Richard M. Fastow
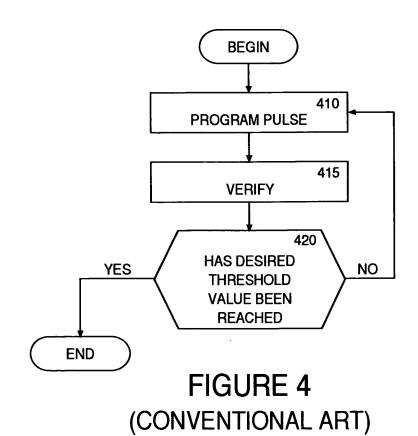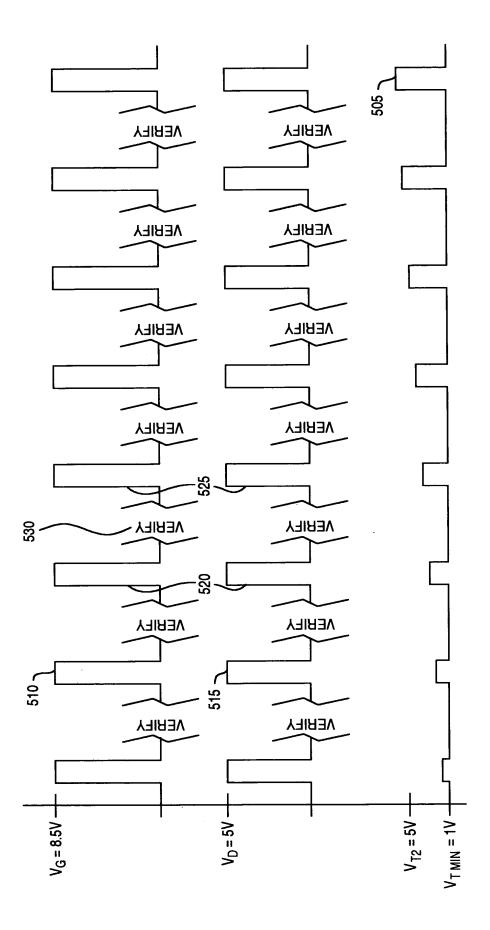USSN: 10/617,971   Attorney Docket #: AMD-H0523

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```
                        ┌─────────┐
                        │  BEGIN  │
                        └─────────┘
                             │
                             ▼
                   ┌──────────────────────┐
                   │                  710 │
                   │  APPLY GATE VOLTAGE  │
                   │  CORRESPONDING TO    │
                   │  DESIRED THRESHOLD   │
                   │  VOLTAGE             │
                   └──────────────────────┘
                     │                  │
              ┌──────┘                  └──────┐
              ▼                                ▼
     ┌─────────────────┐            ┌─────────────────┐
     │            715  │            │            720  │
     │  RAMP DRAIN     │            │  MONITOR DRAIN  │
     │  VOLTAGE        │            │  CURRENT        │
     └─────────────────┘            └─────────────────┘
              │                                │
              └────────────┐       ┌───────────┘
                           ▼       ▼
                   ┌──────────────────────┐
                   │                  725 │
                   │  WHEN DRAIN CURRENT  │
                   │  DROPS, REMOVE DRAIN │
                   │  AND GATE VOLTAGES   │
                   └──────────────────────┘
                             │
                             ▼
                        ┌─────────┐
                        │   END   │
                        └─────────┘
```
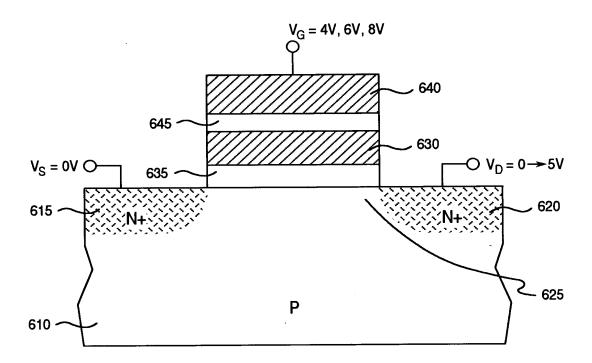
FIGURE 7

TITLE: PROGRAMMING OF A FLASH MEMORY CELL
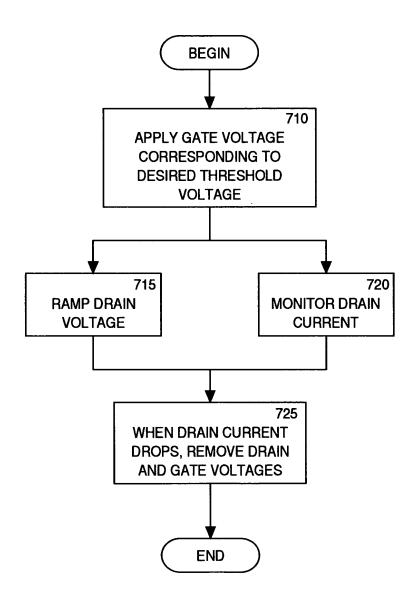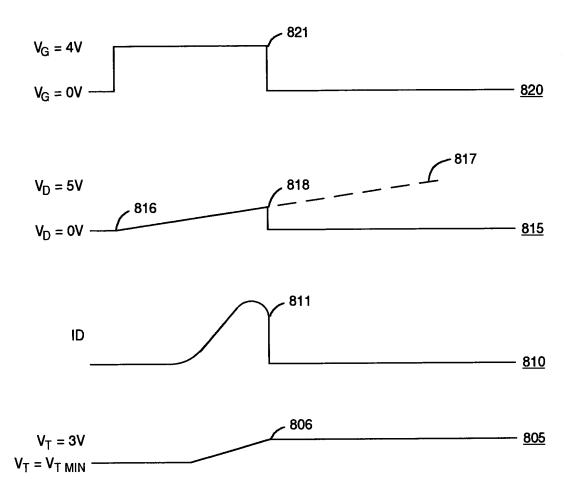INVENTOR(S): Sheung Hee Park, Wing Han Leung, and Richard M. Fastow
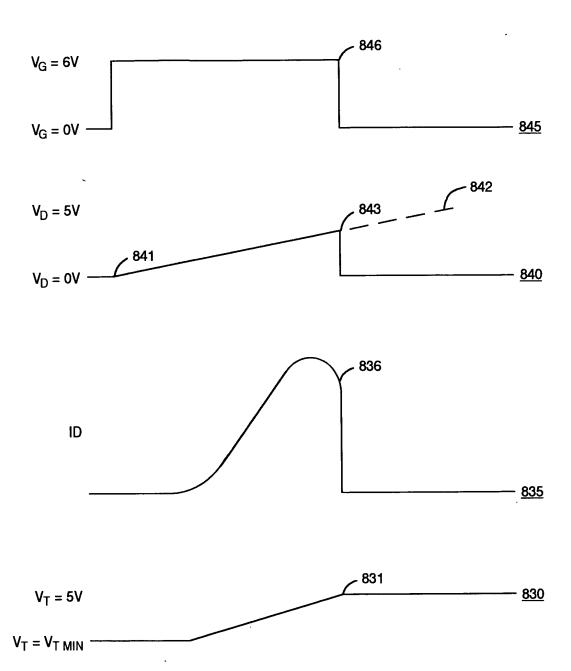USSN: 10/617,971   Attorney Docket #: AMD-H0523

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FIGURE 8A

TITLE: PROGRAMMING OF A FLASH MEMORY CELL
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FIGURE 8B

FIGURE 8C

TITLE: PROGRAMMING OF A FLASH MEMORY CELL
INVENTOR(S): Sheung Hee Park, Wing Han Leung, and Richard M. Fastow
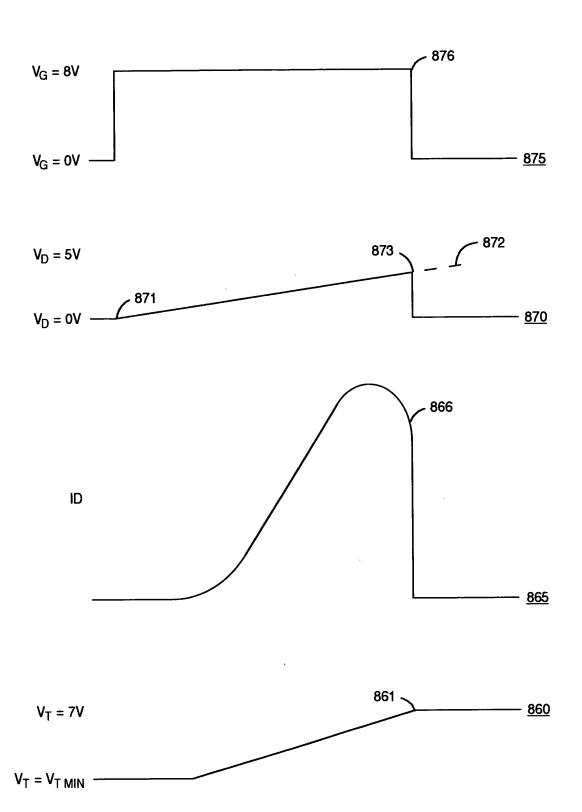USSN: 10/617,971   Attorney Docket #: AMD-H0523

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FIGURE 9